Research article



# Analysis of Duty Cycle, Inductance, and Capacitance Variations on Buck Converter Performance Using PSIM Software

Isra' Nuur Darmawan\*, Kholistianingsih, Slamet Fajar Budhi Nugroho, Nur Johara

Department of Electrical Engineering, Universitas Wijayakusuma Purwokerto, Indonesia

\*Correspondence: isra.nuur.darmawan@unwiku.ac.id

https://doi.org/10.62777/aeit.v2i2.38

Received: 15 October 2024 Revised: 25 July 2025 Accepted: 31 July 2025 Published: 5 October 2025 Abstract: This study investigates the influence of duty cycle, inductance, and capacitance variations on the performance of a buck converter through simulation using PSIM software. The research aims to quantify how these parameters affect output voltage and ripple, which are key factors in achieving efficient and stable DC-DC conversion for renewable energy applications. The converter was modeled with an input voltage of 48 V, an intended output voltage of 24 V, and a switching frequency of 20 kHz. Simulation results show that the output voltage increases linearly with the duty cycle. At a 50% duty cycle, the converter achieved an output voltage of 23.9 V, confirming accurate voltage regulation. Furthermore, ripple voltage was found to decrease significantly with higher inductance and capacitance values, reaching a minimum of 0.1 V when L is 750  $\mu$ H and C is 1,250  $\mu$ F. These results demonstrate that optimizing LC parameters can substantially improve voltage stability and filtering efficiency. The findings provide practical design guidance for highefficiency buck converters used in renewable energy and power electronic applications.



**Copyright:** (c) 2025 by the authors. This work is licensed under a Creative Commons Attribution 4.0 International License.

**Keywords**: buck converter, duty cycle, inductance, capacitance, ripple voltage, PSIM, DC-DC converter

# 1. Introduction

In renewable energy systems, power converters play a vital role in regulating and stabilizing the variable output of energy sources such as wind turbines and photovoltaic modules. The fluctuating voltage generated by these systems must be conditioned before being supplied to batteries or loads to ensure reliability and longevity of the energy storage components [1]. A key element in this conditioning process is the DC–DC converter, which adjusts the voltage level according to system requirements. Among various types, the buck converter, or step-down converter, is widely used to reduce input voltage to a desired lower output level with high efficiency [2].

The output voltage of a buck converter is primarily governed by the duty cycle of the Pulse Width Modulation (PWM) signal that controls the switching device. Therefore, accurate regulation of the duty cycle is essential to maintain stable voltage levels. In addition to the duty cycle, the design of the output filter—typically composed of an

inductor (L) and a capacitor (C)—has a substantial impact on the output voltage quality. Improper selection of these components can result in excessive voltage ripple, reduced efficiency, and potential stress on both active and passive components [3], [4].

Previous studies have focused on control strategies and converter topologies to enhance voltage stability and minimize ripple. However, limited research has quantitatively analyzed the combined effects of duty cycle variation and LC parameter selection on buck converter performance using simulation-based approaches [5], [6], [7]. Understanding these relationships is critical for achieving optimal design parameters, particularly in renewable energy systems where converter stability directly influences system efficiency and reliability.

This study aims to analyze the influence of duty cycle, inductor, and capacitor variations on the output voltage and ripple of a buck converter using PSIM software. The findings are expected to provide design insights for improving voltage regulation and minimizing ripple in DC–DC conversion systems applied to renewable energy technologies.

# 2. Literature Review

### 2.1. Related Works

Several studies have examined the influence of converter parameters on voltage regulation in DC–DC systems. A study reported that increasing the duty cycle proportionally raises the output voltage in small-scale wind turbine controllers, while LC filters effectively reduce voltage ripple [8].

Another investigation analyzed the performance of buck converters for renewable energy applications and found that the selection of inductor—capacitor (LC) parameters significantly affects output voltage stability and switching noise [9]. Other works have focused on control methods, including PID- and PI-based PWM regulation, to enhance converter efficiency [10], [11].

However, most of these studies emphasized control strategies rather than providing a quantitative analysis of LC parameter variation and duty cycle effects on buck converter performance. This research addresses that gap by systematically evaluating how variations in duty cycle, inductance, and capacitance influence output voltage and ripple using PSIM simulation.

### 2.2. DC to DC Converter Overview

A DC–DC converter transforms a fixed DC input voltage into a regulated DC output at a different voltage level. Depending on the conversion direction, converters are categorized as buck (step-down) or boost (step-up) types [12]. Non-isolated converters such as the buck converter are widely applied in renewable energy systems because of their compact design and high efficiency.

### 2.3. Buck Converter

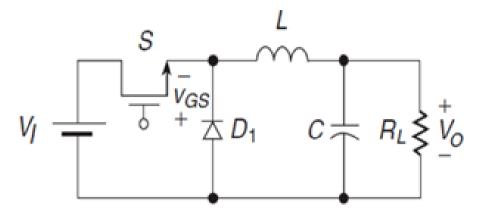
A buck converter operates by periodically switching a semiconductor device (typically a MOSFET) to transfer energy from the input source to the output load through an LC filter. The basic relationship between the output voltage, input voltage, and duty cycle is given by:

$$V_{out} = D \times V_{in} \tag{1}$$

where D represents the fraction of the switching period during which the switch is ON. Equation (1) assumes continuous conduction mode (CCM) and ideal component behavior [13]. Figure 1 shows a buck converter circuit using an LC.

Darmawan et al., Applied Engineering, Innovation, and Technology (2025) vol. 2 no. 2

**Figure 1.** Buck converter circuit using an LC.



### 2.4. Pulse Width Modulation

Pulse Width Modulation (PWM) is used to control the average voltage delivered to the load by adjusting the ON duration of the switching signal while maintaining a constant switching frequency. The duty cycle D can be defined as:

$$D = \frac{T_{on}}{T_{on} + T_{off}} \tag{2}$$

where  $T_{on}$  and  $T_{off}$  denote the switch ON and OFF durations within one complete cycle. An increase in duty cycle results in a proportional increase in the converter's output voltage, as described by Equation (1).

# 2.5. Ripple Voltage and LC Filter Design

In switching converters, output ripple arises due to the periodic charging and discharging of the inductor and capacitor [14]. A properly designed LC filter minimizes the output ripple while maintaining fast transient response. Higher inductance reduces ripple current but increases cost and size; therefore, an optimal balance between component values is essential for achieving efficient converter performance [15].

Existing studies have established that duty cycle and LC filter design both influence converter performance, yet comprehensive simulation-based analysis integrating these parameters remains limited. This work contributes to closing that gap by investigating their combined effects through PSIM simulations under controlled operating conditions.

# 3. Methods

This research was conducted through simulation modeling of a buck converter using PSIM software to analyze the effects of varying the duty cycle, inductor, and capacitor values on output voltage and ripple. The methodology consisted of four main stages: literature review, model design, simulation, and data analysis.

# 3.1. Simulation Setup

The buck converter was designed based on typical parameters used in low-voltage renewable energy applications. The converter specifications are summarized in Table 1. The MOSFET was used as the active switching device, and a diode provided the freewheeling path for current during the switch-OFF period. The output filter consisted of an inductor and a capacitor arranged in series and parallel, respectively.

**Table 1.** Buck converter specification.

Parameter	Symbol	Value
Input voltage	$V_{in}$	48 V
Desired output voltage	$V_{out}$	24 V
Switching frequency	$f_{s}$	20 kHz
Converter power rating	Р	250 W
Peak-to-peak inductor current	$\Delta I_L$	0.8 A
Peak-to-peak ripple voltage	$\Delta V_{out}$	20 mV

### 3.2. Variable Parameters

To evaluate converter behavior under different operating conditions, three primary parameters were varied during the simulations: the duty cycle, the inductor value, and the capacitor value. The duty cycle was adjusted from 10% to 90% in increments of 10%, allowing observation of the voltage-control characteristic across a wide range of PWM ratios. Inductor values were selected at 250  $\mu\text{H}$ , 500  $\mu\text{H}$ , 750  $\mu\text{H}$ , 1000  $\mu\text{H}$ , and 1250  $\mu\text{H}$ , while the corresponding capacitor values were chosen as 250  $\mu\text{F}$ , 500  $\mu\text{F}$ , 750  $\mu\text{F}$ , 1000  $\mu\text{F}$ , and 1250  $\mu\text{F}$ . Each combination of parameters was simulated individually so that the resulting output voltage and ripple could be recorded without interference from other variables. This systematic variation ensured that the impact of each component on converter performance could be isolated and quantified.

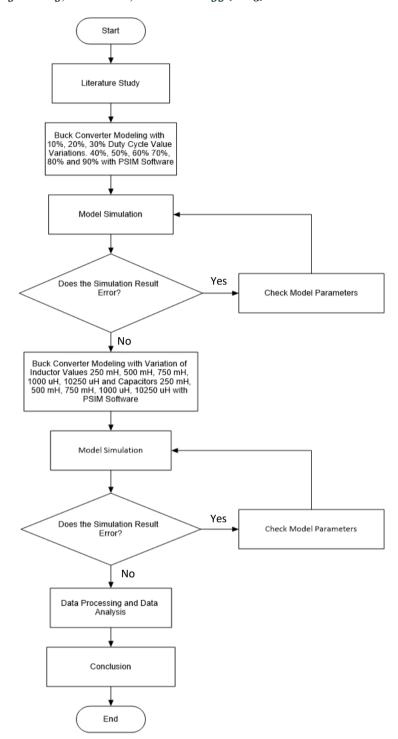
### 3.3. Simulation Process

The simulation procedure began with the creation of an idealized buck-converter circuit in PSIM, incorporating a MOSFET as the main switch and a diode for free-wheeling current. The model parameters—input voltage, switching frequency, and component values—were configured according to the specifications in Table 1. For every test case, the simulation was run until the system reached steady-state operation, after which the output voltage and current waveforms were captured. If any abnormal transients or convergence issues occurred, the parameters were re-checked and the simulation rerun to ensure accuracy. The process followed the sequence illustrated conceptually in Figure 2, which outlines model construction, parameter adjustment, simulation execution, and result validation. Although represented in a flowchart for clarity, the procedure was carried out continuously within the PSIM environment to maintain consistency across all test conditions.

### 3.4. Data Analysis

The recorded waveform data were analyzed to determine both the average output voltage and the magnitude of the output voltage ripple. The ripple amplitude,  $\Delta V_{out}$ , was calculated as the difference between the maximum and minimum voltage values measured during steady-state operation. These results were tabulated to show the dependence of  $V_{out}$  on duty-cycle variation and to evaluate how changes in inductance and capacitance affected the ripple. Graphical representations were subsequently generated to visualize trends and identify optimal parameter combinations. The analysis focused on assessing the linearity of the duty-cycle-to-voltage relationship and quantifying the rate at which ripple decreased with increasing L and C, thereby providing a clear basis for the interpretation presented in Section 4.

Figure 2. Study flowchart.



# 4. Results and Discussion

The simulation was carried out using PSIM to analyze how variations in duty cycle, inductance, and capacitance affect the output voltage and ripple of a buck converter. All simulations were performed with an input voltage of 48 V and a switching frequency of 20 kHz.

# 4.1. Effect of Duty Cycle on Output Voltage

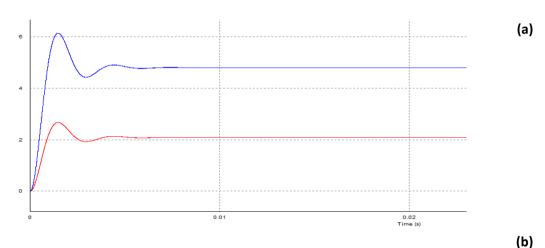
The output voltage was observed for duty cycles ranging from 10% to 90%. Table 2 summarizes the simulated values of output voltage and input current.

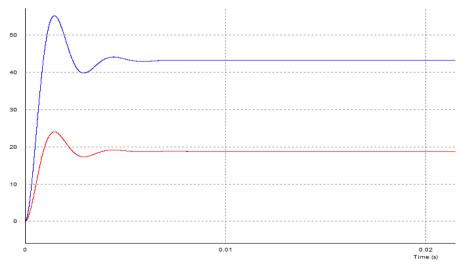
<b>Table 2.</b> Output voltage and input current with varying duty cycle.
---

<b>Duty Cycle</b>	Output Voltage (V)	Input Current (A)
10	4.8	2.0
20	9.6	4.2
30	14.4	6.2
40	19.2	8.3
50	23.9	10.4
60	28.7	12.5
70	33.5	14.6
80	38.3	16.7
90	43.1	18.7

These results show that  $V_{out}$  increases linearly with duty cycle, consistent with the theoretical expression in Equation (1). At a duty cycle of 50 %, the output voltage reaches 23.9 V, closely matching the design target of 24 V. This confirms the accuracy of the PSIM model and validates the control of voltage through PWM modulation. Simulation results on buck converter with duty cycle variation is shown in Figure 3.

Figure 3. Buck converter simulation results with variations in duty cycle: (a) 10%, and (b) 90%. The blue line shows the output voltage, while the red line shows the input current.

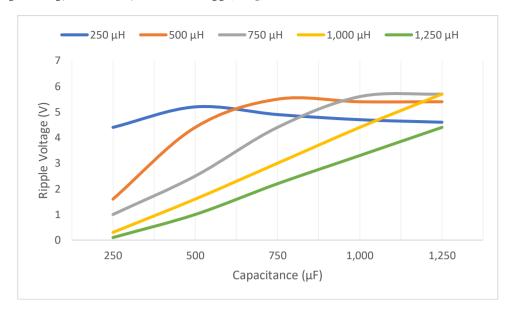




# 4.2. Effect of Inductance and Capacitance on Ripple Voltage

The second set of simulations examined how inductor and capacitor values affect output ripple. The parameters were varied within the inductance between 250–1250  $\mu$ F. Figure 4 presents ripple voltage results by varying the inductance and capacitance.

Figure 4. Buck converter simulation results with varying inductance (250-1,250  $\mu$ H) and capacitance (250-1,250  $\mu$ F).



The simulation results in Figure 4 reveal a non-monotonic dependence of output ripple on capacitance and inductance. For a fixed inductance, increasing capacitance initially reduces ripple, but beyond a certain capacitance, the ripple can increase again. This behavior is consistent with the resonant dynamics of the LC filter: larger capacitance lowers the LC natural frequency. If the natural frequency approaches the switching frequency (or one of its harmonics/subharmonics), the LC network can exhibit peaking and amplify switching components instead of attenuating them. In addition, a very large capacitance combined with low equivalent series resistance (ESR) yields a high-Q filter with little damping, which further increases the likelihood of resonance and observable oscillation. Thus, while moderate increases in C improve ripple attenuation, excessive C (especially without appropriate damping) can shift the system into a resonance region and worsen ripple — an effect clearly visible in the high-C, high-L cells of Figure 4.

### 4.3. Discussion

The simulation results confirm the expected linear relation between output voltage and duty cycle while revealing a more intricate dependence of ripple on LC filter sizing. Moderate increases in capacitance effectively reduce ripple by improving charge storage and lowering voltage fluctuations across the output. However, excessive capacitance can interact with large inductance values to shift the LC resonance close to the 20 kHz switching frequency, producing noticeable ripple amplification. This finding highlights a practical limitation often overlooked in simplified converter analyses: the LC filter cannot be enlarged indefinitely without risking resonance or sluggish dynamic response.

The most favorable operating region in this study lies between  $L=500-750~\mu H$  and  $C=250-750~\mu F$ , where ripple voltage remains below approximately 2.5 V and waveforms exhibit stable steady-state behavior. Component values beyond this range offer diminishing returns in ripple reduction and may introduce instability. These results emphasize that ripple minimization and dynamic stability are coupled design objectives. The data therefore complement classical buck-converter theory by illustrating how real component interactions and filter resonance shape converter performance in practice.

# 5. Conclusions

This study used PSIM to analyze how duty cycle, inductance, and capacitance affect buck-converter performance. Output voltage followed the theoretical linear relation with duty cycle. Ripple behavior was more nuanced: moderate increases in L or C reduced

ripple, but excessive capacitance (particularly when combined with large inductance and low ESR) shifted the LC resonance toward the switching frequency and produced amplified ripple. An optimal design window of approximately between 500–750  $\mu H$  and 250–750  $\mu F$  was identified, balancing attenuation and stability. Future work will incorporate hardware validation to confirm and refine these findings.

Funding: This research received no external funding.

**Data Availability Statement:** The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflicts of Interest: The authors declare no conflicts of interest.

# References

- [1] N. Tayebi, A. A. Najafabadi, M. S. Naderi, A. Khorsandi, and S. H. Hosseinian, "Voltage Regulation in a DC Micrigrid with Renewable Energy Resources, Energy Storage Systems and Electric Vehicles Station using Hierarchical Control Method," in 2023 5th International Conference on Optimizing Electrical Energy Consumption (OEEC), IEEE, Feb. 2023, pp. 35–39. doi: 10.1109/OEEC58272.2023.10135467.
- [2] H.-H. Chou, H.-L. Chen, Y.-H. Fan, and S.-F. Wang, "Adaptive On-Time Control Buck Converter with a Novel Virtual Inductor Current Circuit," *Electronics* (*Basel*), vol. 10, no. 17, p. 2143, Sep. 2021, doi: 10.3390/electronics10172143.
- [3] P. A. Bustaman and T. Abuzairi, "Component Analysis of MOSFET in Synchronous Buck Converter Circuit Using LTspice Simulation," in 2024 International Seminar on Intelligent Technology and Its Applications (ISITIA), IEEE, Jul. 2024, pp. 76–81. doi: 10.1109/ISITIA63062.2024.10668278.
- [4] J.-S. Kim, J.-O. Yoon, and B.-D. Choi, "A High-Light-Load-Efficiency Low-Ripple-Voltage PFM Buck Converter for IoT Applications," *IEEE Trans Power Electron*, vol. 37, no. 5, pp. 5763–5772, May 2022, doi: 10.1109/TPEL.2021.3131594.
- [5] N. Hutagalung, B. W. Dionova, and D. Hendrawati, "Design and Simulation of Asynchronous Buck Converter using Fuzzy Logic Controller (FLC)," *Eksergi*, vol. 20, no. 02, pp. 29–36, May 2024, doi: 10.32497/eksergi.v20i02.5804.
- [6] T. Jiang, S. Zhang, J. Xie, J. Fan, C. Yang, and X. Han, "A Coupled L-LC Filter for Interleaved Buck Converter Ripple Cancellation," *IEEE Trans Power Electron*, vol. 39, no. 5, pp. 6028–6039, May 2024, doi: 10.1109/TPEL.2024.3365171.
- [7] S. Quan and S. Yuan, "Closed-loop Simulation of Buck Converter Based on PSIM," E3S Web of Conferences, vol. 256, p. 02021, May 2021, doi: 10.1051/e3sconf/202125602021.
- [8] R. I. Putri, I. N. Syamsiana, M. Rifa'i, and F. Aditya, "Voltage control for variable speed wind turbine

- using buck converter based on PID controller," *IOP Conf Ser Mater Sci Eng*, vol. 1073, no. 1, p. 012048, Feb. 2021, doi: 10.1088/1757-899X/1073/1/012048.
- [9] B. Yodwong, D. Guilbert, W. Kaewmanee, M. Phattanasak, M. Hinaje, and G. Vitale, "Improved Sliding Mode-Based Controller of a High Voltage Ratio DC–DC Converter for Electrolyzers Supplied by Renewable Energy," *IEEE Transactions on Industrial Electronics*, vol. 71, no. 8, pp. 8831–8840, Aug. 2024, doi: 10.1109/TIE.2023.3322009.
- [10] H. S. Sridhar and K. Sakshith Devaiah, "Modelling and analysis of Voltage Mode control (VMC) of Buck Converter using P, PI, PID Controller," in 2024 International Conference on Smart Systems for applications in Electrical Sciences (ICSSES), IEEE, May 2024, pp. 1–5. doi: 10.1109/ICSSES62373.2024.10561294.
- [11] A. Srikakulam and S. Narayan J, "Application of Normalized Error PI Controller to Higher Order DC-DC Converters," in 2024 2nd International Conference on Cyber Physical Systems, Power Electronics and Electric Vehicles (ICPEEV), IEEE, Sep. 2024, pp. 1–6. doi: 10.1109/ICPEEV63032.2024.10932070.
- [12] X. Weng *et al.*, "Comprehensive comparison and analysis of non-inverting buck boost and conventional buck boost converters," *The Journal of Engineering*, vol. 2019, no. 16, pp. 3030–3034, Mar. 2019, doi: 10.1049/joe.2018.8373.
- [13] L. Tai, M. Lin, J. Wang, and C. Hou, "Synchronous Control Strategy with Input Voltage Feedforward for a Four-Switch Buck-Boost Converter Used in a Variable-Speed PMSG Energy Storage System," Electronics (Basel), vol. 10, no. 19, p. 2375, Sep. 2021, doi: 10.3390/electronics10192375.
- [14] M. P. Varghese, A. Manjunatha, and T. V. Snehaprabha, "The study on the effect of voltage ripple on multiphase buck converters with phase shedding control scheme for SCADA applications," Bulletin of Electrical Engineering and Informatics, vol.

Darmawan et al., Applied Engineering, Innovation, and Technology (2025) vol. 2 no. 2

10, no. 4, pp. 1856–1863, Aug. 2021, doi: 10.11591/eei.v10i4.2798.

**Disclaimer/Publisher's Note:** The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MSD Institute and/or the editor(s). MSD Institute and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.